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UTILITY PATENT APPLICATION TRANSMITTAL LETTER

Attorney Docket No.: SC11100ZP

Mailing Date: June 12, 2000

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To: Assistant Commissioner for Patents
Box Patent Application
Washington D.C., 20231

Dear Sir:

Transmitted herewith for filing under 37 C.F.R. 1.53(b) is a:

☒ New Nonprovisional Utility Patent Application; or

☐ Continuation; or ☐ Divisional; or ☐ Continuation-In-Part (CIP); of prior US Application No. _____, filed on _____, having U.S. Examiner _____, in Group Art Unit _____

Of: William C. Peatman, Eric S. Johnson, and Adolfo C. Reyes

For: **METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND SEMICONDUCTOR COMPONENT THEREOF**

☒ **5** sheets of drawings and **20** pages of specification and claims.

☒ Newly executed oath or declaration combined with Power of Attorney on **3** pages.

☐ Copy of oath or declaration from prior U.S. application serial no. _____
☐ The following named inventor(s) from the prior application are hereby deleted from this application in accordance with 37 C.F.R. 1.63(d)(2) and 1.33(b): _____.

☐ Foreign priority to EPO patent application having serial number _____ and a filing date of _____, is hereby claimed under 35 USC 119.

☒ An Assignment Transmittal Letter and Assignment of the invention to Motorola, Inc.

☒ An Information Disclosure Statement (IDS), with PTO-1449, and 11 citation copies.

☒ Return Receipt Postcard.

☐ Preliminary Amendment.

☐ Please cancel pending claims _____.

☐ Incorporation by Reference (for Continuation/Division/CIP application). The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein. Since the present application is based on a prior US application, please amend the specification by adding the following sentence before the first sentence of the specification:

"The present application is based on prior US application No. _____, filed on_____ _____, which is hereby incorporated by reference, and priority thereto for common subject matter is hereby claimed."

☐ Applicant hereby petitions pursuant to 37 C.F.R. §1.136(a) for a _____ month extension of time for response to the outstanding Official Action mailed _____. The period for response was previously set to elapse _____, and is accordingly hereby extended to _____, which is still within the six-month statutory period for response (35 U.S.C. § 133) which elapses _____. The reason for this petition is that a Division, Continuation, or CIP is being filed, and it is desired to maintain the present application in pending condition pursuant to 35 USC § 120 through at least the filing of the Division, Continuation, or CIP application. The required Extension Fee established by 37 C.F.R. § 1.17(a) pursuant to 35 U.S.C. § 41(a) (8) is:

EXTENSION	FEE
☐ First Month	$110.00
☐ Second Month	$380.00
☐ Third Month	$870.00
☐ Fourth Month	$1,360.00
☐ Fifth Month	$1,850.00

☒ The filing fee is calculated as follows:

CLAIMS AS FILED, LESS ANY CANCELED BY AMENDMENT

FOR	NUMBER OF CLAIMS	NUMBER EXTRA	RATE		FEE
TOTAL CLAIMS	25 - 20 =	5	x $18	=	$ 90.00
INDEPENDENT CLAIMS	3 - 3 =	0	x $78	=	$ 0.00
MULTIPLE DEPENDENT CLAIMS			$260	=	$ 0.00
BASIC FEE				=	$ 690.00
TOTAL FILING FEE				=	$ 780.00

☒ Please charge Deposit Account No. 13-4771 in the amount of $ 780.00 for the Total Filing Fee, and the Extension Fee under 37 C.F.R. §1.136(a), if applicable.

☒ The Commissioner is hereby authorized to charge any additional fees which may be required now or in the future during the entire pendency of this application under 37 C.F.R. 1.16 or 37 C.F.R. 1.17, including any present or future time extension fees which may be required, or credit any overpayment to Deposit Account No. 13-4771.

☒ This sheet is submitted in **duplicate**.

This transmittal letter has 2 total pages.

June 12, 2000
DATE

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METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND SEMICONDUCTOR COMPONENT THEREOF

Field of the Invention

This invention relates, in general, to electronics, and more particularly, to methods of manufacturing semiconductor components and semiconductor components thereof.

Background of the Invention

Heterostructure Insulated Gate Field Effect Transistors (HIGFETs) are well-known to those skilled in the art and are used for a variety of applications including complimentary digital circuits and enhancement mode power amplifier circuits. Some prior HIGFETs are formed by growing a gallium arsenide capping layer of three nanometers over a heterostructure substrate. The heterostructure substrate includes an aluminum gallium arsenide barrier layer over an indium gallium arsenide channel layer, which in turn is located over a conducting semiconductor layer. One problem with these prior HIGFETs is their large variability in output current.

Accordingly, a need exists for a method of manufacturing a semiconductor component and a semiconductor component thereof that has lower variability in direct current (dc) and radio frequency (rf) output currents and has other improved electrical performance characteristics for digital and analog circuit applications.

Brief Description of the Drawings

The invention will be better understood from a reading of the following detailed description, taken in conjunction with the accompanying drawing figures in which:

FIGs. 1, 2, 3, and 4 illustrate cross-sectional views of a semiconductor component during different steps of a manufacturing process in accordance with an embodiment of the invention;

FIG. 5 illustrates a flow chart of a method of manufacturing the semiconductor component illustrated in FIGs. 1, 2, 3, and 4 in accordance with an embodiment of the invention;

FIGs. 6, 7, and 8 illustrate cross-sectional views of another semiconductor component during different steps of another manufacturing process in accordance with an embodiment of the invention; and

FIG. 9 illustrates a flow chart of a method of manufacturing the semiconductor component illustrated in FIGs. 6, 7, and 8 in accordance with an embodiment of the invention.

For simplicity and clarity of illustration, the drawing figures illustrate the general manner of construction, and descriptions and details of well-known features and techniques are omitted to avoid unnecessarily obscuring the invention. Additionally, elements in the drawing figures are not necessarily drawn to scale, and the same reference numerals in different figures denote the same elements.

Furthermore, the terms first, second, third, and the like in the description and in the claims, if any, are used for distinguishing between similar elements and not necessarily for describing a sequential or chronological order. It is further understood that the terms so used are interchangeable under appropriate circumstances. Moreover, the terms over, under, and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing relative positions. It is understood that the terms so used are interchangeable under appropriate circumstances. It is further understood that the embodiments of the invention described herein are capable of being manufactured or operated in other orientations than described or illustrated herein.

Detailed Description of the Drawings

FIGs. 1, 2, 3, and 4 illustrate cross-sectional views of a semiconductor component 100 during different steps of a manufacturing process. In FIG. 1, a substrate 110 is provided with a surface 119. In the preferred embodiment, substrate 110 is a delta-doped, heteroepitaxial semiconductor structure. As an example, substrate 110 can include a support layer 111 comprised of semi-insulating gallium arsenide. Substrate 110 can further include a buffer layer 112 overlaying support layer 111, a doping layer 115 overlaying buffer layer 112, a spacer layer 116 overlying doping layer 115, a channel layer 117 overlaying spacer layer 116, and a barrier layer 118 overlaying channel layer 117.

Buffer layer 112 can be comprised of a single layer or a plurality of layers and can have a thickness of approximately one hundred to three hundred nanometers. Buffer layer 112 can be comprised of gallium arsenide and/or aluminum gallium arsenide. In the preferred embodiment, buffer layer 112 consists essentially of undoped gallium arsenide and is located on support layer 111. As used herein, the term "undoped" is defined as a doping level of less than approximately 1 x 10^{15} atoms per centimeter squared.

Doping layer 115 can be a delta-doped or non-delta-doped layer. As an example, doping layer 115 can be comprised of gallium arsenide delta-doped with a dopant such as, for example, silicon to a doping concentration of approximately 1 x 10^{11} to 5 x 10^{12} atoms per centimeter squared. In the preferred embodiment, doping layer 115 consists essentially of gallium arsenide and silicon and is located on buffer layer 112.

Spacer layer 116 can have a thickness of approximately two to four nanometers. Spacer layer 116 can be comprised of gallium arsenide. In the preferred embodiment, spacer layer 116 consists essentially of undoped gallium arsenide and is located on doping layer 115.

Channel layer 117 can have a thickness of approximately ten to twenty nanometers. Channel layer 117 can be comprised of indium gallium arsenide or another semiconductor. In the preferred embodiment, channel layer 117 is located on spacer layer 116 and consists essentially of indium gallium arsenide having an indium mole fraction of approximately fifteen to twenty percent.

Barrier layer 118 can have a thickness of approximately fifteen to thirty-five nanometers. Barrier layer 118 can be comprised of aluminum gallium arsenide. In the preferred embodiment, barrier layer 118 consists essentially of aluminum gallium arsenide having a high aluminum mole fraction of approximately seventy-five percent. A top surface of barrier layer 118 forms surface 119 for substrate 110 and is located on channel layer 117.

Next, a layer 120 is provided over surface 119 of substrate 110. Layer 120 can be comprised of gallium arsenide. Other equivalent materials that can be used for layer 120 include indium gallium nitride, indium gallium phosphide, and indium gallium aluminum phosphide. In the preferred embodiment, layer 120 consists essentially of undoped gallium arsenide. As an example, layer 120 can have a thickness of approximately three to twelve nanometers. In the preferred embodiment, layer 120 has a thickness of approximately six to nine nanometers. Also, in the preferred embodiment, layer 120 is located on surface 119 of substrate 110.

Next, a gate contact 210 is formed over layer 120. In the preferred embodiment, gate contact 210 is located on layer 120. As illustrated in FIG. 1, gate contact 210 covers a first portion of layer 120 and is absent over a second portion of layer 120.

As an example, gate contact 210 can be formed using the following process. First, a metal layer is formed over layer 120. As an example, the metal layer can have a thickness of approximately three hundred to five hundred nanometers and can consists essentially of titanium tungsten nitride, titanium tungsten, titanium, or tungsten. Next, an etch mask can be formed over the metal layer. As an example, the etch mask can be comprised of photoresist. The metal layer can be etched using a dry etch process, and then the etch mask can be removed. The etching or patterning of the metal layer forms gate contact 210 over the first portion of layer 120 and also over a first portion of surface 119 of substrate 110. The etching or patterning of the metal layer also exposes the second portion of layer 120.

Turning to FIG. 2, substrate 110 is illustrated in simplified form and does not show the plurality of layers described in FIG. 1. As illustrated in FIG. 2, the second portion of layer 120 is removed. As an example, the second portion of layer 120 can be removed using a wet etchant comprised of citric acid monohydrate, hydrogen peroxide, and water. The removal of the second portion of layer 120 after forming gate contact 210 exposes a second portion of surface 119 of substrate 110. This removal process keeps the first portion of layer 120 underneath gate contact 210. Furthermore, this first portion of layer 120 preferably remains undoped.

Then, an electrically insulating layer 220 is formed over gate contact 210, layer 120, and surface 119 of substrate 110. In the preferred embodiment, layer 220 is formed on gate contact 210 and surface 119 of substrate 110. Layer 220 can be comprised of a dielectric material such as silicon oxide, silicon nitride, or silicon oxy-nitride. In the preferred embodiment, layer 220 is comprised of silicon nitride that is deposited using a high frequency chemical vapor deposition process. As an example, layer 220 can have a thickness of approximately twenty to sixty nanometers.

Next, lightly doped source region 231 and lightly doped drain region 232 can be formed in substrate 110 after removing the second portion of layer 120. As an example, regions 231 and 232 can be implanted through layer 220 and into surface 119 of substrate 110. Furthermore, regions 231 and 232 can be defined by an implant mask comprised of photoresist or can be defined using the remaining portion of layer 120 as the implant mask. In the preferred embodiment, regions 231 and 232 have an n-type conductivity and extend from surface 119 of substrate 110 into buffer layer 112 (FIG. 1) of substrate 110, but do not extend into support layer 111 (FIG. 1) of substrate 110.

Subsequently, turning to FIG. 3, a source region 311 and a drain region 312 can be formed in substrate 110 after removing the second portion of layer 120. As an example, regions 311 and 312 can be implanted through layer 220 and into surface 119 of substrate 110 and can be defined by an implant mask comprised of photoresist. Similar to lightly doped source and drain regions 231 and 232, source and drain regions 311 and 312 preferably extend from surface 119 of substrate 110 into buffer layer 112 (FIG. 1) of substrate 110, but preferably do not extend into support layer 111 (FIG. 1) of substrate 110.

Next, a spacer 340 can be formed adjacent to gate contact 210 after removing the second portion of layer 120. Spacer 340 can be comprised of a single layer, but is preferably comprised of multiple layers. As an example of a multi-layered spacer, a first electrically insulating layer 320 can be formed over layer 220, and then a second electrically insulating layer 330 can be formed over layer 320. Layers 320 and 330 can be comprised of different dielectric materials. In the preferred embodiment, layer 320 is comprised of aluminum nitride, and layer 330 is comprised of tetra-ethyl-ortho-silicate (TEOS), which is a form of silicon oxide. As an example, layer 320 can have a thickness of approximately twenty to forty nanometers, and layer 330 can have a thickness

of approximately three hundred to four hundred nanometers. Next, layer 330 can be etched anisotropically with a dry etchant, and then layer 320 can be etched isotropically with a wet etchant.

Then, regions 231, 232, 311, and 312 in substrate 110 are annealed. In the preferred embodiment, this annealing step occurs after removing the second portion of layer 120 and also occurs after forming layer 220. The anneal process activates the dopants in regions 231, 232, 311, and 312, and the annealing process also increases the density of layer 220 to protect substrate 110.

Subsequently, electrical isolation regions 350 are formed in substrate 110. As an example, regions 350 can be implanted through layer 220 and into surface 119 of substrate 110 and can be defined by an implant etch mask comprised of photoresist. In the preferred embodiment, regions 350 extend from surface 119 of substrate 110 into support layer 111 (FIG. 1) of substrate 110.

Referring to FIG. 4, an electrically insulating layer 410 is formed over spacer 340 and layer 220. As an example, layer 410 can be comprised of a dielectric material. In the preferred embodiment, layer 410 is comprised of silicon dioxide and can have a thickness of approximately one hundred to four hundred nanometers.

Next, source contact via 421 and drain contact via 422 are formed in layer 410, layer 220, and substrate 110. In the preferred embodiment, vias 421 and 422 extend into layers 118, 117, 116, 115, and 112 (FIG. 1) of substrate 110, but preferably do not extend into layer 111 (FIG. 1) of substrate 110.

Next, source contact 431 and drain contact 432 are formed in source contact via 421 and drain contact via 422, respectively, and over source region 311 and drain region 312, respectively. Source and drain contacts 431 and 432 are ohmic contacts. In the preferred embodiment,

contacts 431 and 432 are comprised of nickel, germanium, and gold and are patterned using a lift-off process. After the lift-off process defines contacts 431 and 432, a high-temperature step anneals contacts 431 and 432. Subsequent manufacturing steps form at least one interconnect layer electrically coupled to contacts 431 and 432 and also to gate contact 210.

FIG. 5 illustrates a flow chart of a method 500 of manufacturing semiconductor component 100 illustrated in FIGs. 1, 2, 3, and 4. At a step 510 of method 500 in FIG. 5, a substrate with a surface is provided. Next, at a step 520 in method 500, a layer comprised of undoped gallium arsenide is provided over the surface of the substrate. At a step 530, a gate contact is formed over a first portion of the layer, and at a step 540, a second portion of the layer is subsequently removed to expose a portion of the surface of the substrate. Subsequently, at a step 550, an electrically insulating layer is formed over the gate contact and the substrate, and at a step 560, source and drain regions are formed in the substrate. Then, at a step 570, a spacer is formed adjacent to the gate contact, and at a step 580, the source and drain regions are annealed. Next, at a step 590 of method 500, source and drain contacts are formed over the source and drain regions.

Electrical tests of semiconductor components manufactured using the method described in FIGs. 1, 2, 3, 4, and 5 show many improvements. For example, the standard deviation of the channel sheet resistance in the semiconductor components is greatly reduced, and the standard deviation of the output current of the semiconductor components are also greatly reduced. Additionally, the semiconductor components have lower gate leakage currents. Furthermore, the turn-on voltage for these semiconductor components is higher, which allows for larger input and output, dc and rf power levels. The dc and rf output currents, and thus the dc and rf power, of these semiconductor components can also be increased by increasing the delta-doping

concentration in the substrate. This increase in output current can be accomplished while maintaining the breakdown voltage by adjusting the implant profiles of the lightly doped source and drain regions and the source and drain regions.

FIGs. 6, 7, and 8 illustrate cross-sectional views of a semiconductor component 600 during different steps of another manufacturing process. Component 600 is a different embodiment of component 100 in FIGs. 1, 2, 3, and 4. As illustrated in FIG. 6, component 600 includes substrate 110, layer 120, and gate contact 210. However, the second portion of layer 120 is not etched or removed right after forming gate contact 210. Instead, layer 220 is formed over gate contact 210 and layer 120 before removing the second portion of layer 120. Furthermore, lightly doped source and drain regions 231 and 232 and source and drain regions 311 and 312 are formed in substrate 110 before removing the second portion of layer 120. Then, spacer 340 is formed adjacent to gate contact 210 before removing the second portion of layer 120.

After forming regions 231, 232, 311, and 312 in substrate 110 and after forming spacer 340, the second portion of layer 120 is removed. This removal process first involves removing an overlying portion of layer 220 and then removing the second portion of layer 120. As illustrated in FIG. 7, the first portion of layer 120 remains underneath gate contact 210 after removing the second portion of layer 120, and a third portion of layer 120 remains underneath spacer 340 after removing the second portion of layer 120.

Then, an electrically insulating layer 710 is formed over spacer 340, gate contact 210, and the remaining portions of layer 120. As an example, layer 710 can be similar to layer 220, but layer 710 preferably has a thickness greater than that of layer 220. Next, regions 231, 232, 311,

and 312 are annealed. This anneal process also increases the density of layer 710. Subsequently, electrical isolation regions 350 are formed in substrate 110.

Turning to FIG. 8, electrically insulative layer 410 is deposited, and source and drain contact vias 421 and 422 are also formed. Next, source and drain contacts 431 and 432 are formed within vias 421 and 422, and contacts 431 and 432 are annealed.

FIG. 9 illustrates a flow chart of a method 900 of manufacturing semiconductor component 600 illustrated in FIGs. 6, 7, and 8. At a step 910 of method 900 in FIG. 9, a substrate is provided with a surface. At a step 920 of method 900, a layer comprised of semi-insulting gallium arsenide is provided over the surface of the substrate. At a step 930, a gate contact is formed over a first portion of the layer. Next, at a step 940, source and drain regions are formed in the substrate, and at a step 950, a spacer is formed adjacent to the gate contact. Then, at a step 960, a second portion of the layer is removed. Next, at a step 970, an electrically insulating layer is formed over the gate contact and the substrate, and at a step 980, the source and drain regions are annealed. Subsequently, at a step 990 of method 900, source and drain contacts are formed over the source and drain regions.

Therefore, an improved method of manufacturing a semiconductor component and semiconductor component thereof are provided to overcome the disadvantages of the prior art. The semiconductor components have improved electrical performance characteristics including greatly reduced variations in sheet resistance, dc and rf output currents, and breakdown voltage. Furthermore, the semiconductor components may have higher turn-on voltages and lower gate leakage currents. The semiconductor components additionally have well-controlled, positive threshold voltages, which is very well suited for digital and analog circuit applications.

Although the invention has been described with reference to specific embodiments, it will be understood by those skilled in the art that various changes may be made without departing from the spirit or scope of the invention. For instance, the numerous details set forth herein such as, for example, chemical concentrations, material compositions, and layer thicknesses are provided to facilitate the understanding of the invention and are not provided to limit the scope of the invention. Accordingly, the disclosure of embodiments of the invention is intended to be illustrative of the scope of the invention and is not intended to be limiting. It is intended that the scope of the invention shall be limited only to the extent required by the appended claims.

CLAIMS

1. A method of manufacturing a semiconductor component comprising:

providing a substrate with a surface;

providing a layer comprised of undoped gallium arsenide over the surface of the substrate;

forming a gate contact over a first portion of the layer; and

removing a second portion of the layer to expose a portion of the surface of the substrate.

2. The method of claim 1 wherein:

providing the layer further comprises providing the layer with a thickness of approximately three to twelve nanometers.

3. The method of claim 1 wherein:

providing the layer further comprises providing the layer with a thickness of approximately six to nine nanometers.

4. The method of claim 1 wherein:

forming the gate contact further comprises exposing the second portion of the layer.

5. The method of claim 1 wherein:

removing the second portion of the layer exposes a portion of the substrate.

6. The method of claim 1 further comprising:

implanting source and drain regions into the substrate after removing the second portion of the layer.

7. The method of claim 1 further comprising:

implanting source and drain regions into the substrate before removing the second portion of the layer.

8. The method of claim 1 further comprising:

forming a spacer adjacent to the gate contact after removing the second portion of the layer.

9. The method of claim 1 further comprising:

forming a spacer adjacent to the gate contact before removing the second portion of the layer.

10. The method of claim 9 further comprising:

keeping a third portion of the layer underneath the spacer after removing the second portion of the layer.

11. The method of claim 1 wherein:

providing the substrate further comprises providing a delta-doped, heteroepitaxial semiconductor structure for the substrate.

12. The method of claim 1 wherein:

providing the substrate further comprises:

providing a support layer;

providing a buffer layer overlying the support layer;

providing a doping layer overlying the buffer layer;

providing a spacer layer overlying the doping layer;

providing a channel layer overlying the spacer layer; and

providing a barrier layer overlying the channel layer.

13. The method of claim 1 wherein:

forming the gate contact further comprises:

forming the gate contact on the layer.

14. The method of claim 1 further comprising:

implanting source and drain regions into the substrate;

annealing the source and drain regions after removing the second portion of the layer; and

forming source and drain contacts over the source and drain regions after removing the second portion of the layer.

15. The method of claim 1 wherein:

removing the second portion of the layer further comprises keeping the first portion of the layer underneath the gate contact; and

removing the second portion of the layer further comprises keeping the first portion of the layer undoped.

16. A method of manufacturing a semiconductor component comprising:

providing a delta-doped, heteroepitaxial semiconductor substrate with a surface, the delta-doped, heteroepitaxial semiconductor substrate comprising:

a support layer comprised of semi-insulating gallium arsenide;

a buffer layer comprised of undoped gallium arsenide overlying the support layer;

a doping layer delta-doped with silicon and overlying the buffer layer;

a spacer layer comprised of undoped gallium arsenide and overlying the doping layer;

an channel layer comprised of indium gallium arsenide and overlying the spacer layer; and

a barrier layer comprised of aluminum gallium arsenide and overlying the channel layer, the barrier layer forming the surface for the delta-doped, heteroepitaxial semiconductor substrate;

providing an undoped gallium arsenide capping layer having a thickness of approximately three to twelve nanometers and overlying the surface of the delta-doped, heteroepitaxial semiconductor substrate;

forming a gate contact over the undoped gallium arsenide capping layer, the gate contact covering a first portion of the undoped gallium arsenide capping layer and absent over a second portion of the undoped gallium arsenide capping layer;

removing the second portion of the undoped gallium arsenide capping layer after forming the gate contact to expose a portion of the surface of the delta-doped, heteroepitaxial semiconductor substrate;

forming a spacer adjacent to the gate contact;

forming source and drain regions in the delta-doped, heteroepitaxial semiconductor substrate; and

forming source and drain contacts over the source and drain regions after removing the second portion of the undoped gallium arsenide capping layer.

17. The method of claim 16 wherein:

forming the source and drain regions further comprises implanting the source and drain regions into the delta-doped, heteroepitaxial semiconductor substrate after removing the second portion of the undoped gallium arsenide capping layer; and

forming the spacer further comprises forming a multi-layered spacer adjacent to the gate contact after removing the second portion of the undoped gallium arsenide capping layer.

18. The method of claim 16 further comprising:

forming the source and drain regions further comprises implanting source and drain regions into the delta-doped, heteroepitaxial semiconductor substrate before removing the second portion of the undoped gallium arsenide capping layer;

forming the spacer further comprises forming a multi-layered spacer adjacent to the gate contact before removing the second portion of the undoped gallium arsenide capping layer; and

keeping a third portion of the undoped gallium arsenide capping layer underneath the multi-layered spacer after removing the second portion of the undoped gallium arsenide capping layer.

19. The method of claim 16 wherein:

providing the undoped gallium arsenide capping layer further comprises providing the undoped gallium arsenide capping layer with a thickness of approximately six to nine nanometers.

20. The method of claim 16 wherein:

providing the delta-doped, heteroepitaxial semiconductor substrate further comprises:

providing the buffer layer on the support layer and consisting essentially of gallium arsenide;

providing the doping layer on the buffer layer and consisting essentially of silicon and gallium arsenide;

providing the spacer layer on the doping layer and consisting essentially of gallium arsenide;

providing the channel layer on the spacer layer and consisting essentially of indium gallium arsenide; and

providing the barrier layer on the channel layer and consisting essentially of aluminum gallium arsenide;

providing the undoped gallium arsenide capping layer further comprises:

providing the undoped gallium arsenide capping layer on the barrier layer;

forming the gate contact further comprises:

forming the gate contact on the first portion of the undoped gallium arsenide capping layer; and

removing the second portion of the undoped gallium arsenide capping layer further comprises:

removing the second portion of the undoped gallium arsenide capping layer to expose a portion of the barrier layer.

21. The method of claim 20 further comprising:

annealing the source and drain regions after removing the second portion of the undoped gallium arsenide capping layer,

wherein:

providing the undoped gallium arsenide capping layer further comprises providing the undoped gallium arsenide capping layer with a thickness of approximately six to nine nanometers.

22. A semiconductor component comprising:

a substrate with a surface;

a layer comprised of undoped gallium arsenide over a first portion of the surface of the substrate; and

a gate contact over the layer,

wherein:

the layer is absent over a second portion of the substrate.

23. The semiconductor component of claim 22 wherein:

the layer has a thickness of approximately six to nine nanometers.

24. The semiconductor component of claim 22 wherein:

the layer has a thickness of approximately three to twelve nanometers; and

the substrate is a delta-doped, heteroepitaxial semiconductor substrate comprising:

a support layer comprised of semi-insulating gallium arsenide;

a buffer layer comprised of gallium arsenide overlying the support layer;

a doping layer delta-doped with silicon and overlying the buffer layer;

a spacer layer comprised of gallium arsenide and overlying the doping layer;

an channel layer comprised of indium gallium arsenide and overlying the spacer layer; and

a barrier layer comprised of aluminum gallium arsenide and overlying the channel layer, the barrier layer forming the surface for the delta-doped, heteroepitaxial semiconductor substrate.

25. The semiconductor component of claim 24 further comprising:

source and drain regions in the substrate;

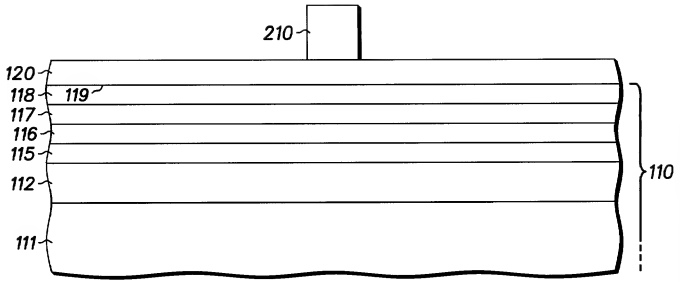
a multi-layered spacer adjacent to the gate contact; and

source and drain contacts overlying the source and drain regions.

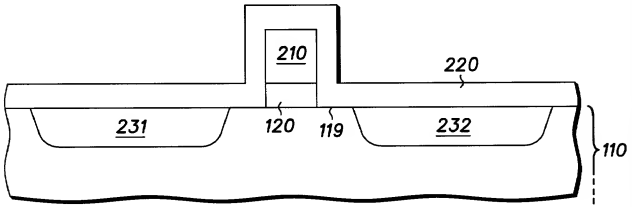
METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND SEMICONDUCTOR COMPONENT THEREOF

Abstract of the Disclosure

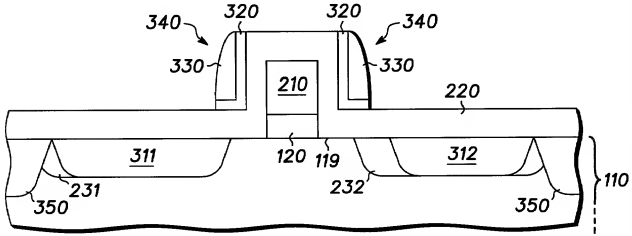
A method of manufacturing a semiconductor component includes providing a substrate (110) with a surface (119), providing a layer (120) of undoped gallium arsenide over the surface of the substrate, forming a gate contact (210) over a first portion of the layer, and removing a second portion of the layer.



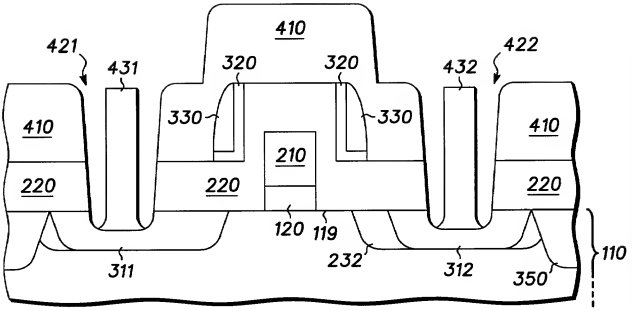
100 FIG. 1



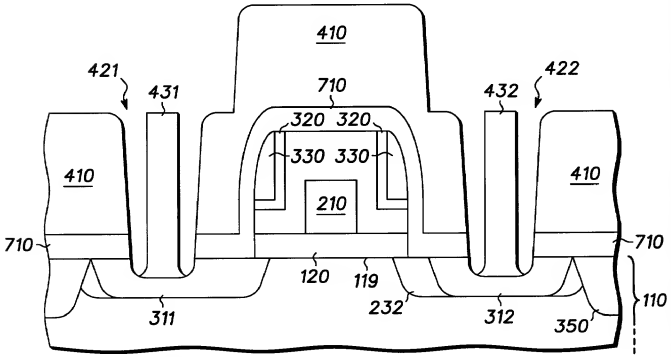
100 FIG. 2



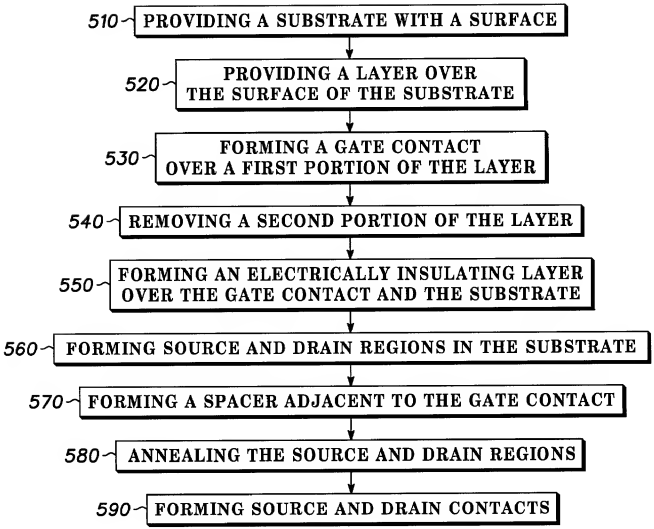
100 FIG. 3



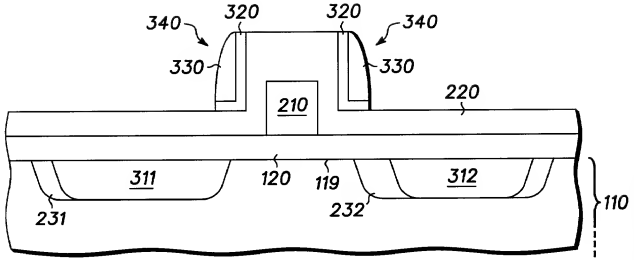
100 FIG. 4



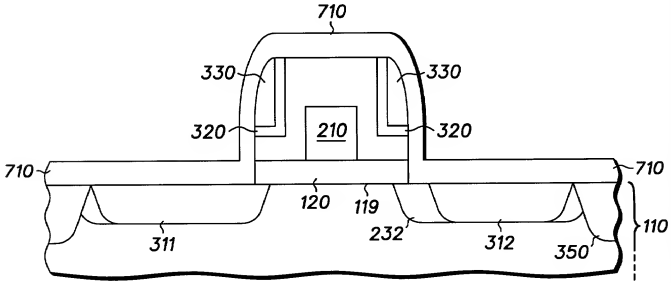
600 FIG. 8


510
PROVIDING A SUBSTRATE WITH A SURFACE
520
PROVIDING A LAYER OVER THE SURFACE OF THE SUBSTRATE
530
FORMING A GATE CONTACT OVER A FIRST PORTION OF THE LAYER
540
REMOVING A SECOND PORTION OF THE LAYER
550
FORMING AN ELECTRICALLY INSULATING LAYER OVER THE GATE CONTACT AND THE SUBSTRATE
560
FORMING SOURCE AND DRAIN REGIONS IN THE SUBSTRATE
570
FORMING A SPACER ADJACENT TO THE GATE CONTACT
580
ANNEALING THE SOURCE AND DRAIN REGIONS
590
FORMING SOURCE AND DRAIN CONTACTS

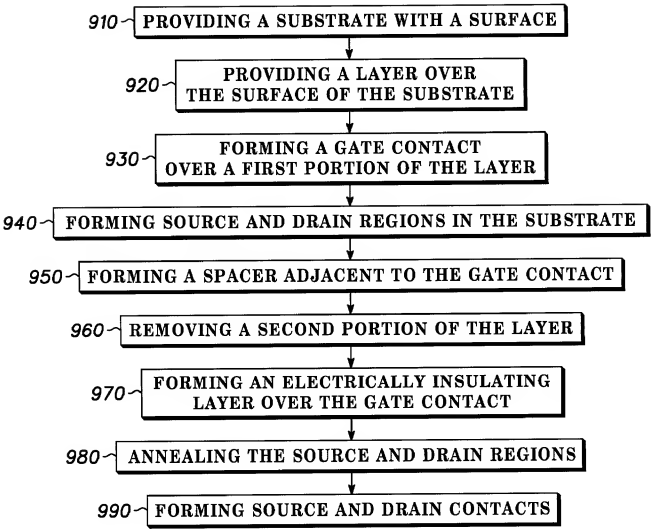
500 FIG. 5



600 FIG. 6



600 FIG. 7



900 FIG. 9

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

Attorney Docket SC11100ZP

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below), or an original, first and joint inventor (if plural names are listed below), of the subject matter which is claimed and for which a patent is sought on the invention entitled METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND SEMICONDUCTOR COMPONENT THEREOF, the specification of which is attached hereto unless the following box is checked:

☐ Application was filed on _____
as Application No. _____
and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or 365(b) any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐ Yes ☐ No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code, § 119 of any United States provisional application(s), listed below:

_____ (Application Number)	_____ (Filing Date)
_____ (Application Number)	_____ (Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below:

(U.S. Parent Application Number or PCT Parent No.)	(Filing Date)	(Country)
(U.S. Parent Application Number or PCT Parent No.)	(Filing Date)	(Country)

I hereby appoint the attorney(s) and/or agent(s) associated with Customer Number 23330 to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Address all telephone calls to Ms. A. Kate Huffman at telephone no. (480) 441-4817.

Address all correspondence to customer number 23330.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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